PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q78894
Sung-kyu CHOI	
Appln. No.: 10/758,040	Group Art Unit: 2111
Confirmation No.: 6125	Examiner: Christopher E. LEE
Filed: January 16, 2004	

For: APPARATUS AND METHOD FOR CONNECTING PROCESSOR TO BUS

REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.41, Appellant respectfully submits this Reply Brief in response to the Examiner's Answer dated January 11, 2008. Entry of this Reply Brief is respectfully requested.

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STATUS OF CLAIMS

Claims 1-10 are all the claims pending in the application and the subject of this appeal. Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bourke et al. (U.S. Patent No. 5,509,124, hereafter "Bourke") in view of Barrenscheen et al. (U.S. Patent Application Publication No. 2003/0084226, hereafter "Barrenscheen"). Claims 2-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki et al. (JP 2000-92365A, hereafter "Masayuki") in view of Barrenscheen. Claims 7-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen, and further in view of Sodos (U.S. Patent No. 5,239,651). Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen and Luo et al. (U.S. Patent No. 6,265,885, hereafter "Luo"). All of the claims are set forth in the attached Appendix.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Rejection of claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Bourke in view of Barrenscheen.

(2) Rejection of claims 2-6 under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen.

Rejection of claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen and Luo.

ARGUMENT

In addition to the arguments set forth in the Appeal Brief filed November 2, 2007, Appellant responds to certain points made in the Examiner's Answer as follows:

As noted in the Appeal Brief, the Examiner appears to unreasonably broadly construe the claimed multiplexer to allegedly read on the bus interface (BI1) of FIG. 4 of Barrenscheen.

In response to Appellant's argument that the Bus Interface BI1 is not a multiplexer, but is merely used to connect the data transmission device DTU to the first through fourth buses BUS1-BUS4, respectively, and consequently, Bus Interface BI1 does not perform the functions of, and is not described as a multiplexer in Barrenscheen, the Examiner asserts in part:

> Barrenscheen is clearly suggesting that the claimed subject matter "**multiplexer**" (i.e., being equalized to **Bus Interface BI1** in Fig. 4) receives first data from a processor (e.g., Module BU11 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) and transfers the received first data to a first memory (e.g., Module BU12 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) through a synchronous data bus (i.e., BUS1 in Figs.2A-B) synchronized with the processor (See Barrenscheen, paragraph [0035], lines 11-12; for example, DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A, wherein said Module BU11 should be synchronized with said BUS1 for said DMA data writing operation), or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor…In other words, the recited claiming language "multiplexer," and its function in the exemplary claim 1 are interpreted as the bus

> interface BI1 performs the same functions of and is described as the claimed subject matter "multiplexer" in Barrenscheen.[1]

However, as is clearly understood by those of ordinary skill in the art, a bus is simply a parallel circuit that connects the major components, or various functional units, of a computer, allowing the transfer of electric impulses from one connected component to any other, or an electrical conductor that makes a common connection between several circuits. A multiplexer is a device which permits the simultaneous transmission of two or more trains of signals or messages over a single channel (as acknowledged by the Examiner).

Appellant respectfully submits that there is simply no teaching or suggestion in Barrenscheen that the Bus Interface, BI1, simultaneously transmits two or more trains of signals or messages over a single channel. Even if Barrenscheen discloses that the Bus Interface receives and transmits data, Barrenscheen does not teach or suggest that the Bus Interface simultaneously transmits two or more trains of signals or messages over a single channel. Accordingly, the Bus Interface cannot function as, or be interpreted as a multiplexer.

As further noted in the Appeal Brief with respect to independent claim 1, Appellant respectfully submitted that there is simply no disclosure in Barrenscheen that the BUS1 is synchronized with a processor, and that paragraph [0035] of Barrenscheen, which the Examiner alleged as disclosing this feature of claim 1 merely discloses that when the data transmission device (DTU) is used as a DMA controller, it can transmit data between devices connected to the

[1] Pages 17-18 of the Examiner's Answer.

same bus or between devices connected between different buses autonomously, and does not require BUS1 and BUS2 be synchronized with the processor.

In response, the Examiner asserts:

> This disclosure in Barrenscheen inherently anticipates that the Modules BU11 or BU21 as a processor sends DMA (Direct Memory Access)command for the DMA operation (e.g., data bursting) to the DTU via the bus BUS1 or BUS2 in Fig. 3, which is clearly teaching said busses BUS1 and BUS2 should be synchronized with said Modules BU11 and BU21 because said Modules BU11 and BU21 should be able to communicate with said DTU for said DMA operation being performed among synchronized components.[2]

Appellant respectfully disagrees with the Examiner's position, and submits that the Examiner now appears to be changing the original rejection by now asserting that this feature of the claims is **"inherent"**.

The standard of teaching required of a prior art reference to support a 35 U.S.C. § 103 rejection is substantially more than to support a 35 U.S.C. § 102 rejection of anticipation, however, since the Doctrine of Inherency does not extend beyond anticipation. Inherency of an advantage and its obviousness are different questions; that which may be inherent is not necessarily known; obviousness cannot be predicated on that which is unknown. *In re Adams*, 53 CCPA 996, 356 F.2d 998, 148 U.S.P.Q. 742 (1966). Inherency and obviousness are entirely different concepts. *In re Rinehart*, 531 F.2d 1048, 189 U.S.P.Q. 143 (CCPA 1976).

[2] Page 19 of the Examiner's Answer.

Inherency and obviousness are distinct concepts. A retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of the elements in the particular claimed combination. In deciding that a novel combination would have been obvious, there must be a supporting teaching in the prior art; for that which may be inherent is not necessarily known, and obviousness cannot be predicated on what is unknown. *See In re Newell*, 13 U.S.P.Q.2d 1248, 1250 (Fed. Cir. 1989).

"In relying upon the theory of inherence, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex Parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & inter. 1990). See M.P.E.P. § 2112.

Applicant respectfully submits that the features of claim 1 which require that the multiplexer receive first data from a processor and transfer the received first data to a first memory through a synchronous data bus synchronized with the processor, do not necessarily flow from the teachings of Barrenscheen and Barrenscheen simply does not teach or suggest that the BUS1 is synchronized with a processor.

As noted in the Appeal Brief, Appellant respectfully submits that the Examiner's assertion that Masayuki teaches both a synchronous bus and an asynchronous bus as required by independent claims 2, 4, and 10 and the submission by the Examiner that bus 34 and bus 33 of Masayuki as allegedly respectively reading on the claimed synchronous and asynchronous buses is erroneous. The Examiner merely assumes that CPU bus 34 is (synchronous) synchronized

with CPU 41, and that image data bus 33 is (asynchronous) not synchronized with CPU 41 because image data bus 33 is not directly connected to CPU 41 in Fig. 2.

In response, the Examiner admits that "FIG. 2 of Masayuki cannot definitely state the operating status, i.e., synchronized or not synchronized with the processor, in detail".[3] Nevertheless, the Examiner maintains that Bus 34 is synchronized with CPU 41 and Bus 34 is not synchronized with the CPU.

The Examiner further seems to assert that several interfaces are needed for interfacing between the image bus and the CPU of Masayuki, and accordingly, this allegedly means that the image data bus is not synchronized with the CPU. Appellant respectfully submits that the Examiner's position is clearly erroneous since the state of a bus - whether it is synchronous or asynchronous - has nothing to do with whether interfaces are connected between the bus and a CPU.

Appellant also respectfully submits that it appears that the image bus 33 is synchronized with CPU 41 as CPU bus 34, because the image bus 33 is directly connected to the CPU bus 34, not via a buffer, as illustrated in FIG. 2 of Masayuki. Therefore, the Examiner's assertion that image bus 33 is an asynchronous data bus not synchronized with the processor and synchronized with the sink generator is clearly erroneous.

In the Appeal Brief, Appellant further noted that the fact that Masayuki teaches a signal processing unit which prevents delay of image data does not necessarily mean that this

[3] Page 21 of the Examiner's Answer.

"inherently" teaches that the image data bus is synchronized with the CPU as alleged by the Examiner.[4]

In response, the Examiner cites paragraph [0036] of Masayuki as allegedly disclosing this feature of the claim. However, this cited portion of Masayuki merely discloses that a memory controller 22 performs data transfer to mediation of the image data bus 33, control of write/read of the image data between the image data memory 32 and each circuit. Nowhere does this cited portion (or any other portion) of Masayuki teach or suggest "an asynchronous bus not synchronized with the processor", as recited in the claims. Appellant respectfully submits that the claimed "synchronous bus" and "asynchronous bus" are simply not taught nor suggested by the cited references.

Further, the term "interface" generally means the communication boundary between two entities, such as a piece of software, a hardware device, or a user. The term "buffer" means a region of memory used to temporarily hold data while it is being moved from one place to another. (refer to "http://en.wikipedia.org/") From these general definitions, Appellant respectfully submits that "interfaces" in Masayuki does **not** provide the function of temporarily holding data for the asychronous communication with the CPU 41.

In other words, the memory interface 27, the host interface 31, and the JPEG interface 30 in Masayuki provide only the functions of connecting such enities as a memory, host, and JPEG with another entity such as the CPU 41 independent of the image data bus 33. Therefore,

[4] Page 19 of the Office Action dated January 18, 2007.

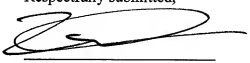
Appellant respectfullly submits that the "buffer" in the present invention does not correspond to the "inferfaces" in Masayuki

In view of the foregoing, Appellant respectfully submits that the rejection of claims 1-20 should be reversed.

CONCLUSION

For the above reasons as well as the reasons set forth in Appeal Brief, Appellant respectfully requests that the Board reverse the Examiner's rejections of all claims on Appeal. An early and favorable decision on the merits of this Appeal is respectfully requested.

Respectfully submitted,



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